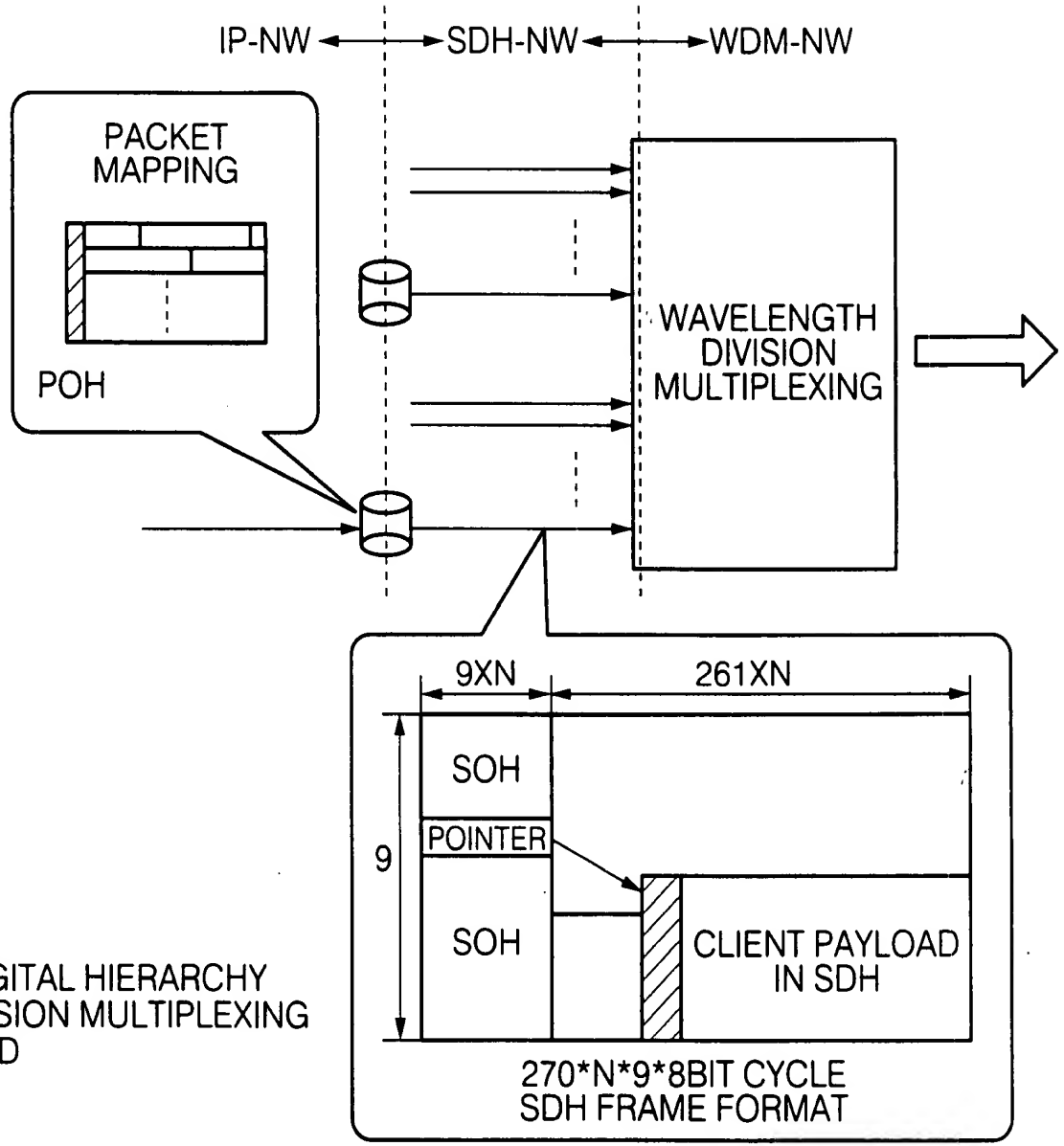
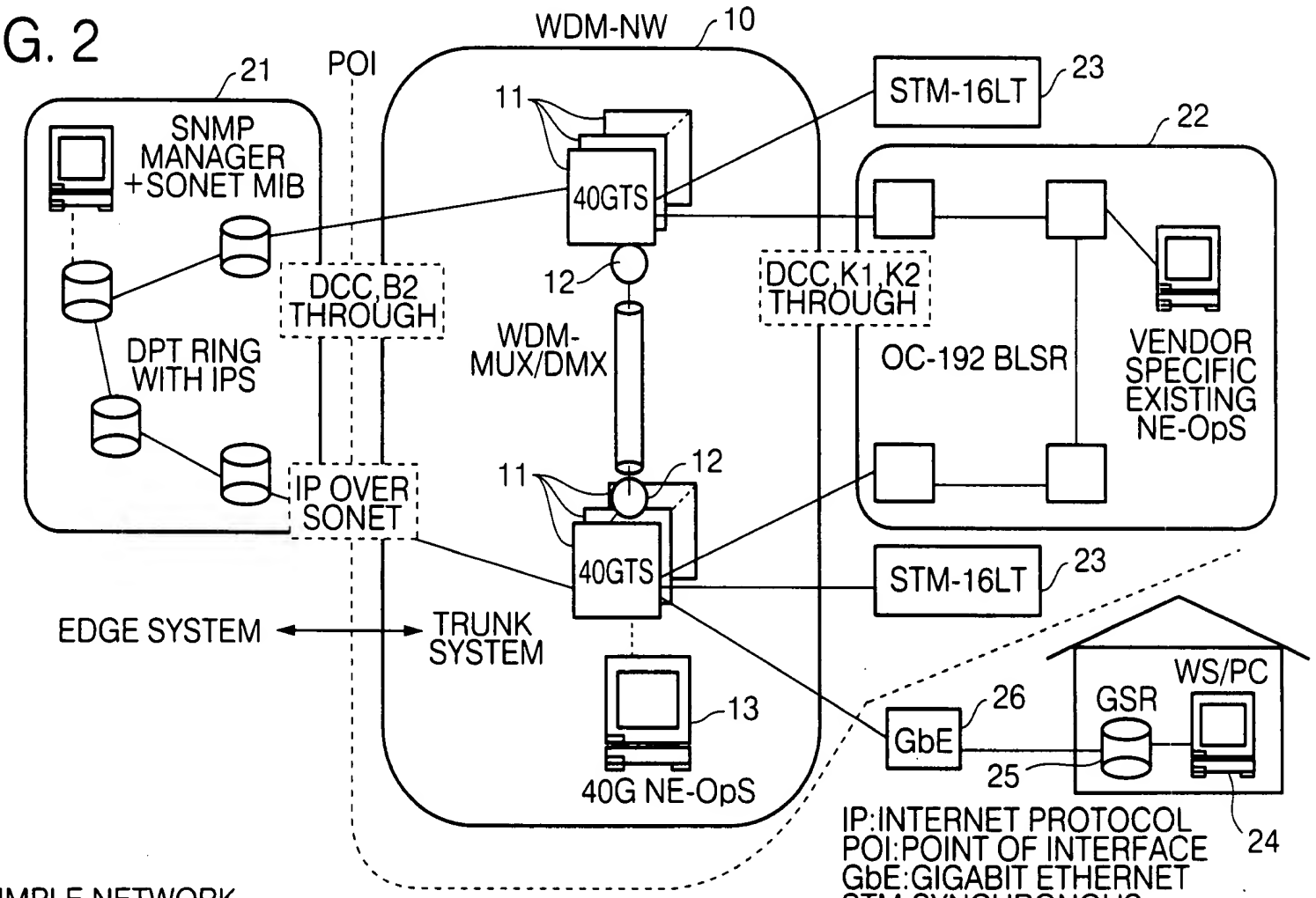
FIG. 1



IP:INTERNET PROTOCOL
SDH:SYNCHRONOUS DIGITAL HIERARCHY
WDM:WAVELENGTH DIVISION MULTIPLEXING
SOH:SECTION OVERHEAD
POH:PATH OVERHEAD

FIG. 2

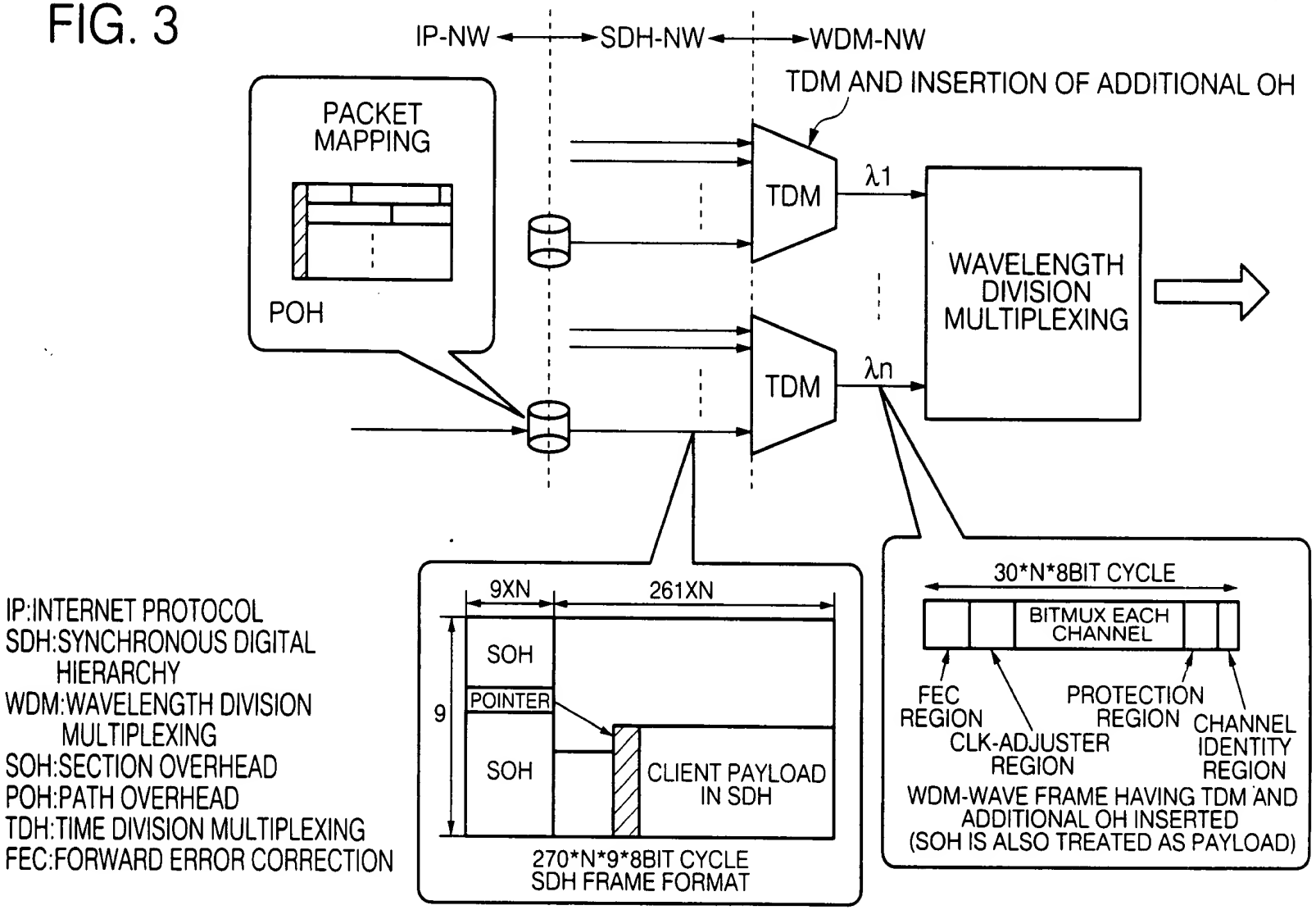


SNMP:SIMPLE NETWORK MANAGEMENT PROTOCOL
SONET:SYNCHRONOUS OPTICAL NETWORK
MIB:MANAGEMENT INFORMATION BASE
DPT:DYNAMIC PACKET TRANSFER

IPS:INTELLIGENT PROTECTION SWITCHING
40GTR:40 GIGABIT/S TDM SYSTEM
DCC:DATA COMMUNICATION CHANNEL

IP:INTERNET PROTOCOL
POI:POINT OF INTERFACE
GbE:GIGABIT ETHERNET
STM:SYNCHRONOUS TRANSPORT MODULE
BLSR:BIDIRECTIONAL LINE SWITCHED RING
LT:LINE TERMINATING EQUIPMENT
GSR:GIGABIT SWITCHED ROUTER

FIG. 3



IP:INTERNET PROTOCOL
SDH:SYNCHRONOUS DIGITAL HIERARCHY
WDM:WAVELENGTH DIVISION MULTIPLEXING
SOH:SECTION OVERHEAD
POH:PATH OVERHEAD
TDH:TIME DIVISION MULTIPLEXING
FEC:FORWARD ERROR CORRECTION

FIG. 4

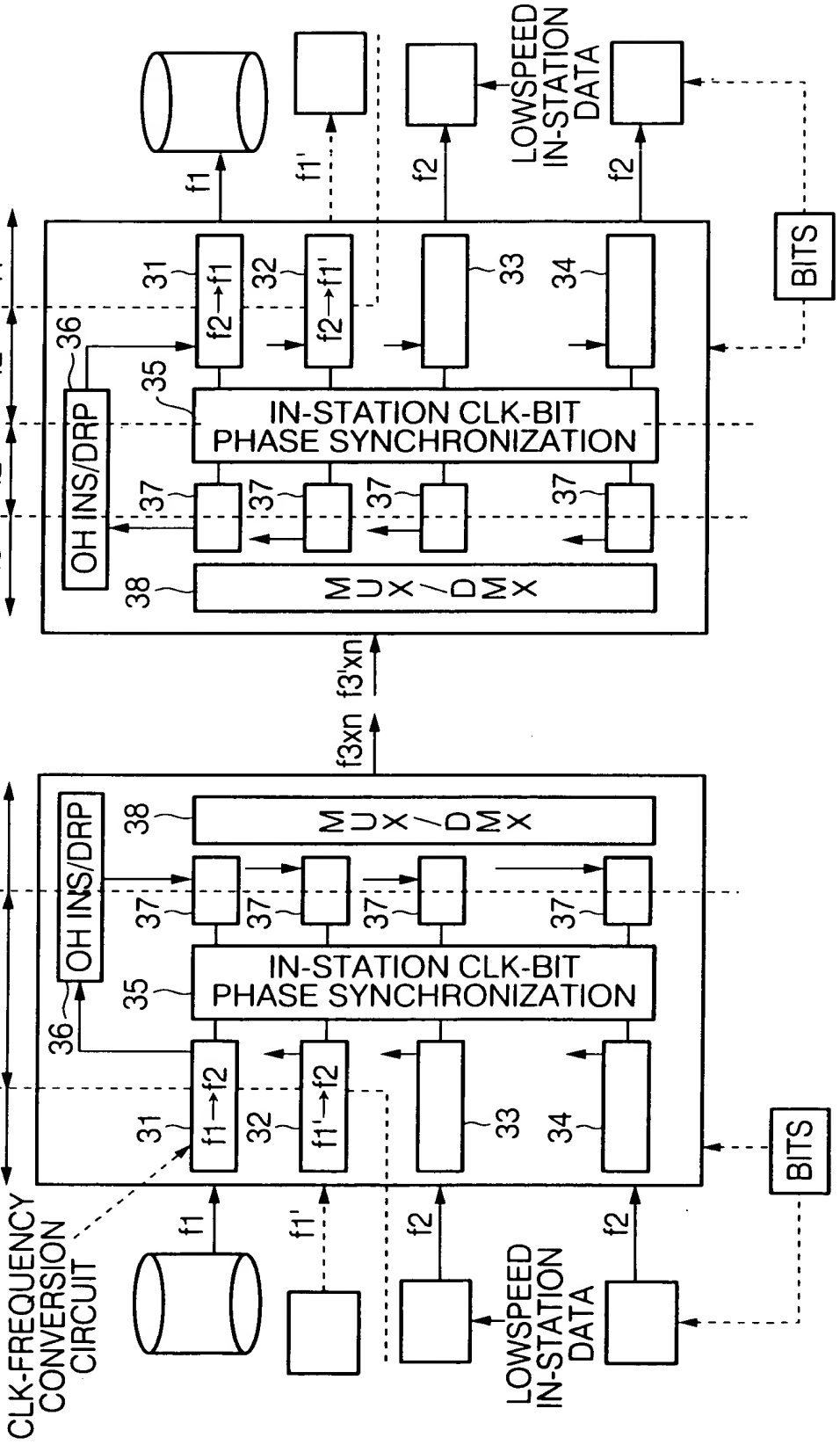
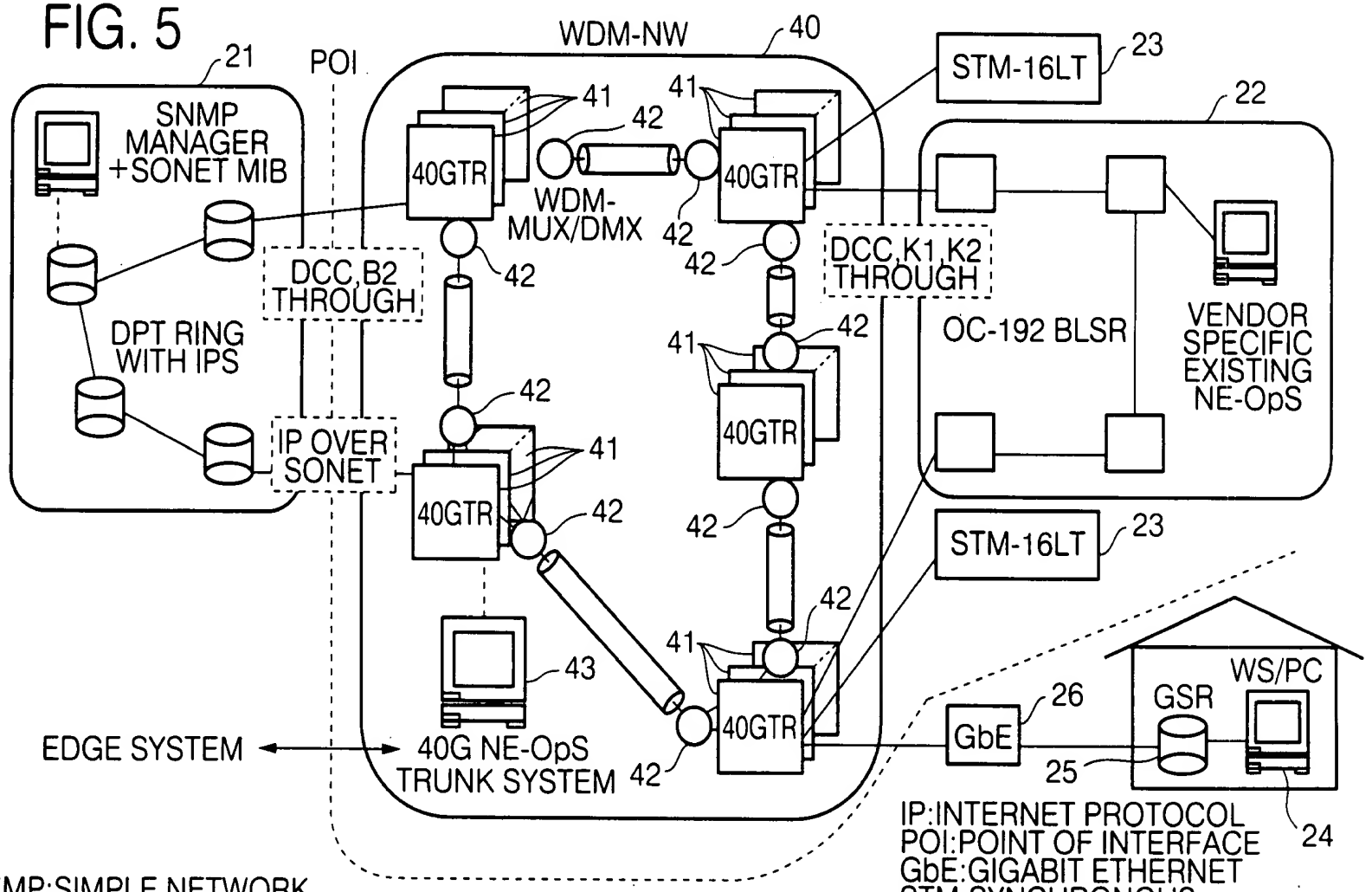

CLK-FREQUENCY CONVERSION CIRCUIT
f1
f1'
f2
LOWSPEED IN-STATION DATA
BITS
f3
f2
f2'
f3'
f1→f2
f1'→f2
f2→f1
f2→f1'
OH INS/DRP
IN-STATION CLK-BIT PHASE SYNCHRONIZATION
MUX/DMX
f3xn
f3'xn
31
32
33
34
35
36
37
38

FIG. 5



SNMP:SIMPLE NETWORK MANAGEMENT PROTOCOL
SONET:SYNCHRONOUS OPTICAL NETWORK
MIB:MANAGEMENT INFORMATION BASE
DPT:DYNAMIC PACKET TRANSFER

IPS:INTELLIGENT PROTECTION SWITCHING
40GTR:40 GIGABIT/S TDM RING SYSTEM
DCC:DATA COMMUNICATION CHANNEL

IP:INTERNET PROTOCOL
POI:POINT OF INTERFACE
GbE:GIGABIT ETHERNET
STM:SYNCHRONOUS TRANSPORT MODULE
BLSR:BIDIRECTIONAL LINE SWITCHED RING
LT:LINE TERMINATING EQUIPMENT
GSR:GIGABIT SWITCHED ROUTER

FIG. 6

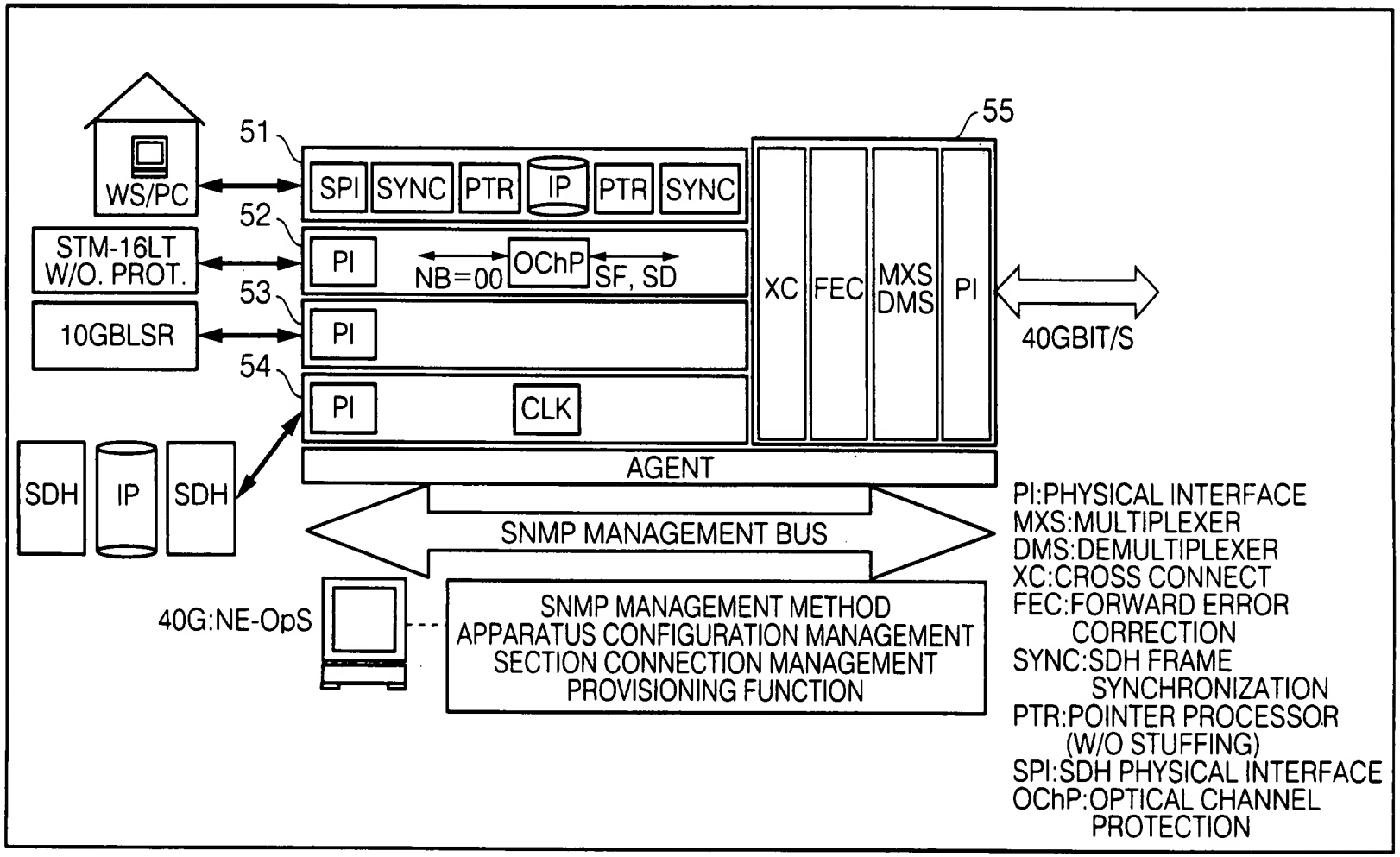

WS/PC
51
SPI
SYNC
PTR
IP
PTR
SYNC
55
52
STM-16LT
W/O. PROT.
PI
NB=00
OChP
SF, SD
XC
FEC
MXS
DMS
PI
40GBIT/S
53
10GBLSR
PI
54
PI
CLK
SDH
IP
SDH
AGENT
SNMP MANAGEMENT BUS
40G:NE-OpS
SNMP MANAGEMENT METHOD
APPARATUS CONFIGURATION MANAGEMENT
SECTION CONNECTION MANAGEMENT
PROVISIONING FUNCTION
PI:PHYSICAL INTERFACE
MXS:MULTIPLEXER
DMS:DEMULTIPLEXER
XC:CROSS CONNECT
FEC:FORWARD ERROR
CORRECTION
SYNC:SDH FRAME
SYNCHRONIZATION
PTR:POINTER PROCESSOR
(W/O STUFFING)
SPI:SDH PHYSICAL INTERFACE
OChP:OPTICAL CHANNEL
PROTECTION

FIG. 7

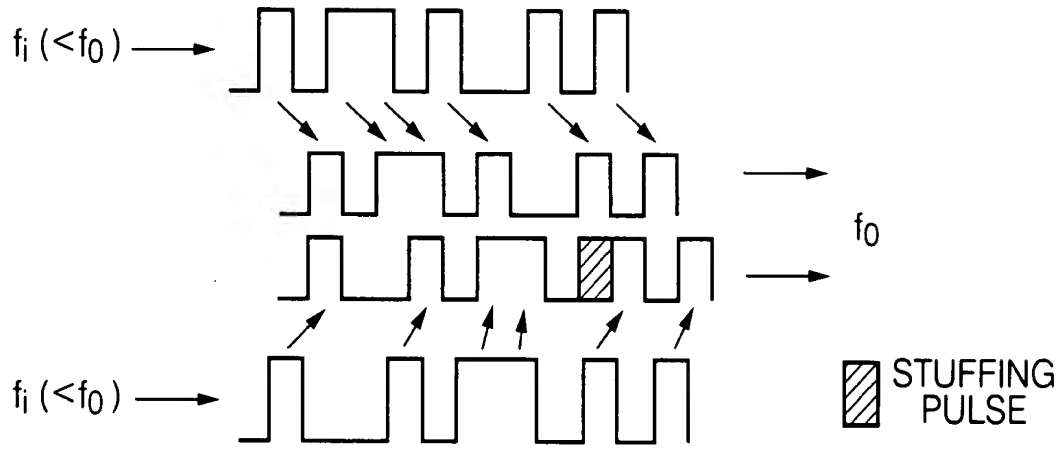


FIG. 8

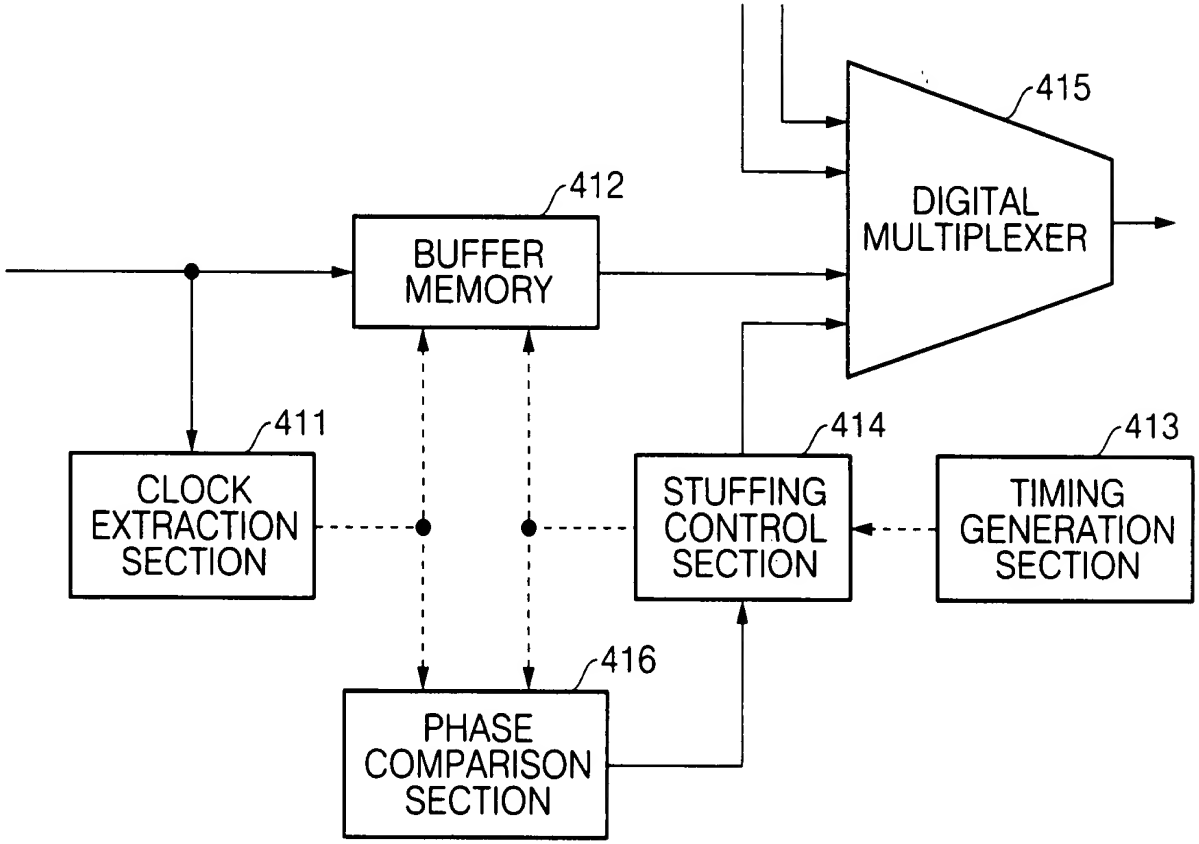

415
412
DIGITAL MULTIPLEXER
BUFFER MEMORY
411
414
413
CLOCK EXTRACTION SECTION
STUFFING CONTROL SECTION
TIMING GENERATION SECTION
416
PHASE COMPARISON SECTION

FIG. 9

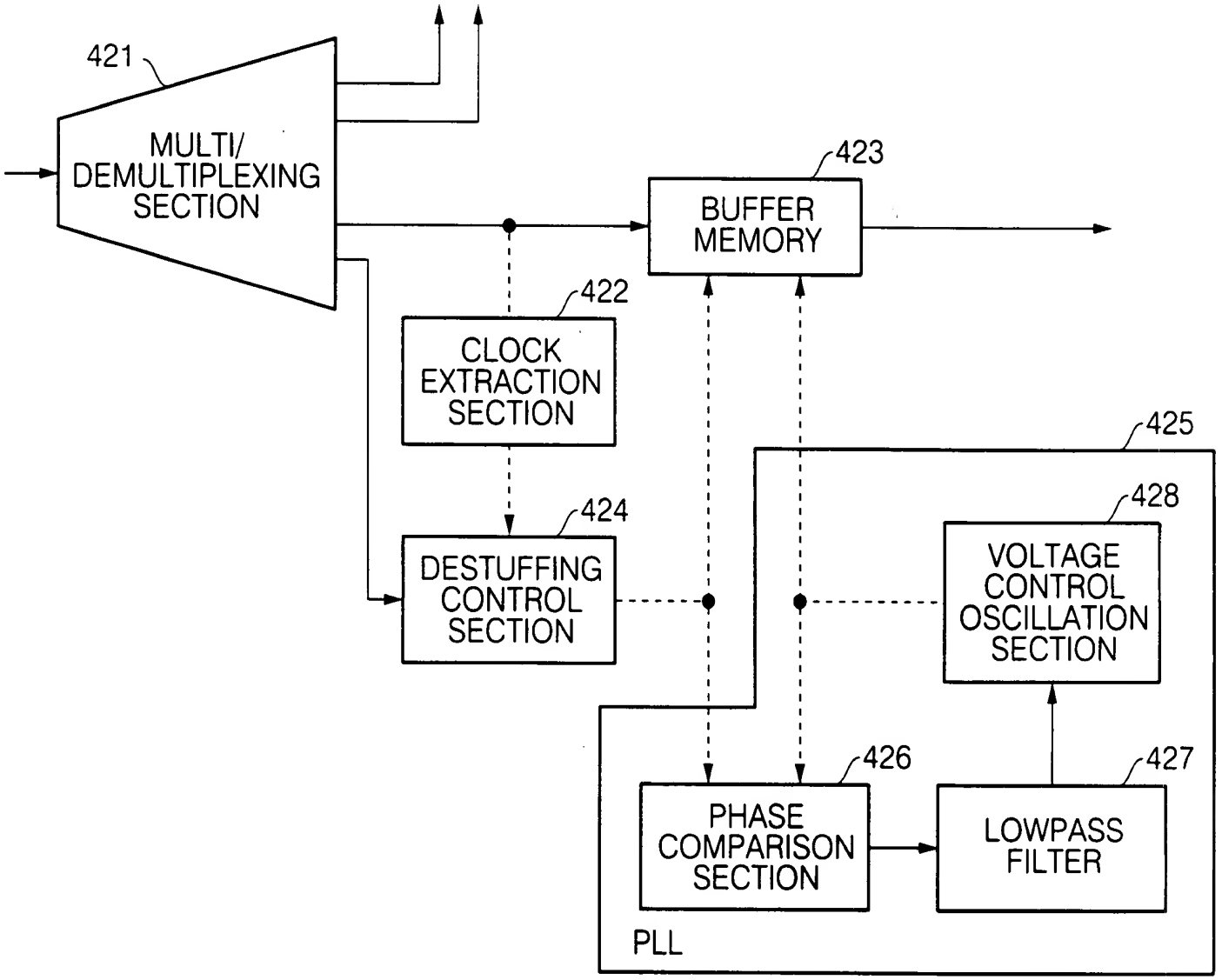

421
MULTI/
DEMULTIPLEXING
SECTION
423
BUFFER
MEMORY
422
CLOCK
EXTRACTION
SECTION
425
424
DESTUFFING
CONTROL
SECTION
428
VOLTAGE
CONTROL
OSCILLATION
SECTION
426
427
PHASE
COMPARISON
SECTION
LOWPASS
FILTER
PLL

FIG. 10

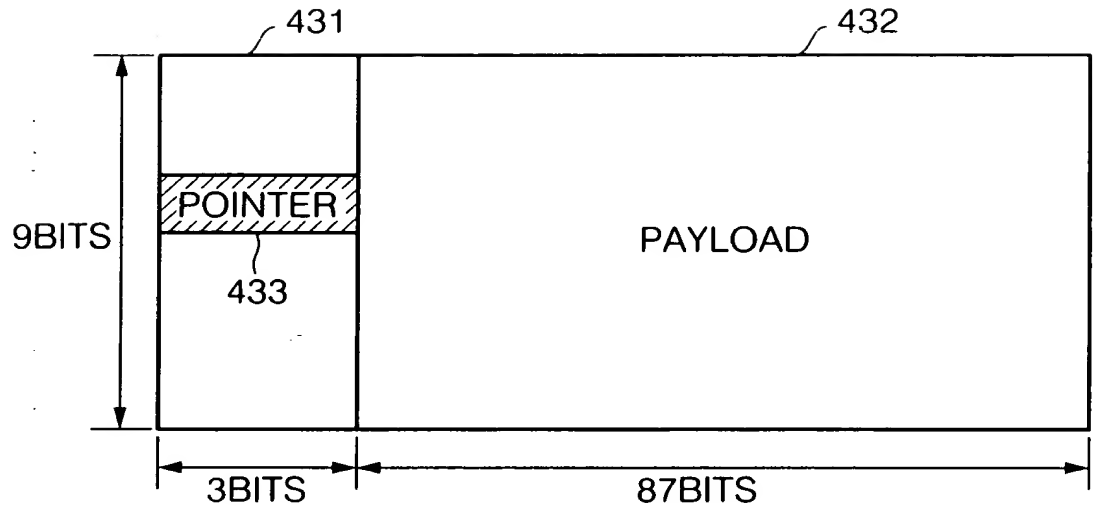

431
432
9BITS
POINTER
433
PAYLOAD
3BITS
87BITS

FIG. 11

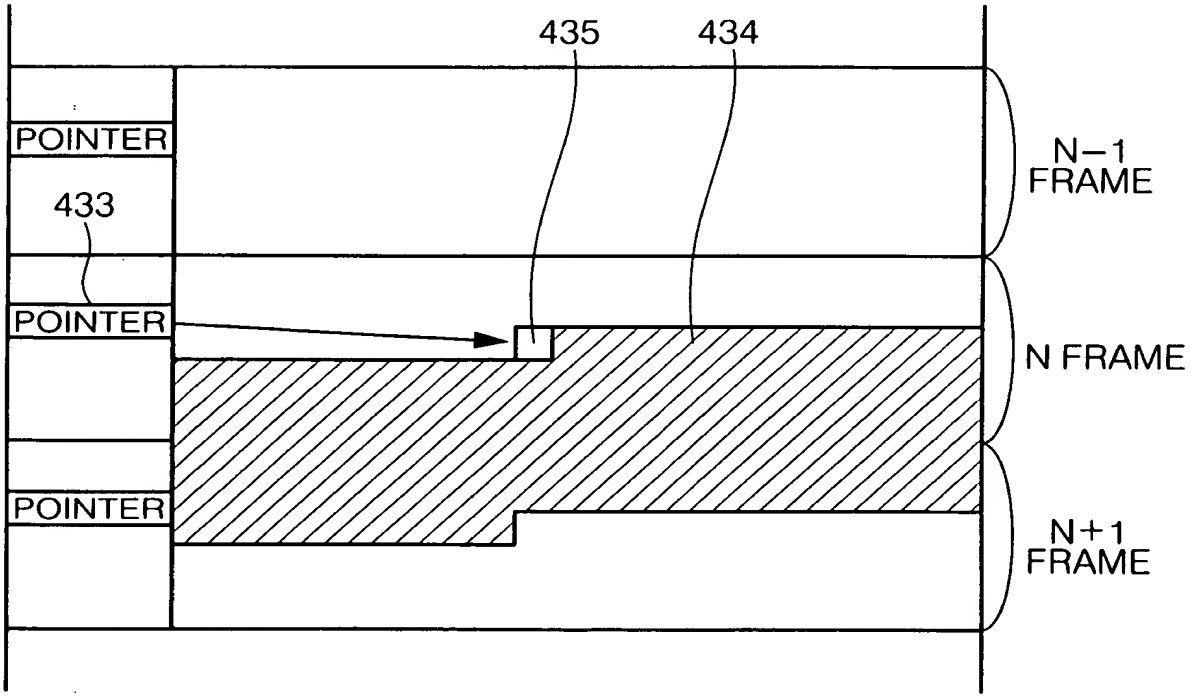

435
434
POINTER
433
POINTER
POINTER
N−1 FRAME
N FRAME
N+1 FRAME

FIG. 12

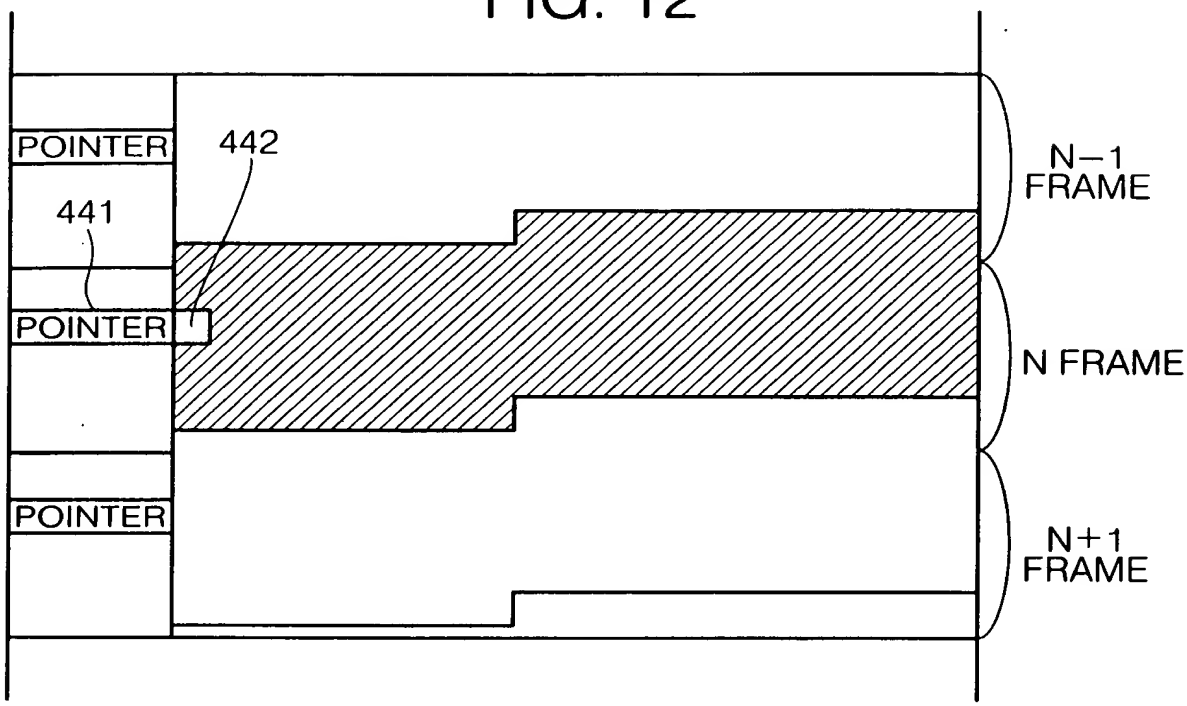

POINTER
442
441
POINTER
POINTER
N−1
FRAME
N FRAME
N+1
FRAME

FIG. 13

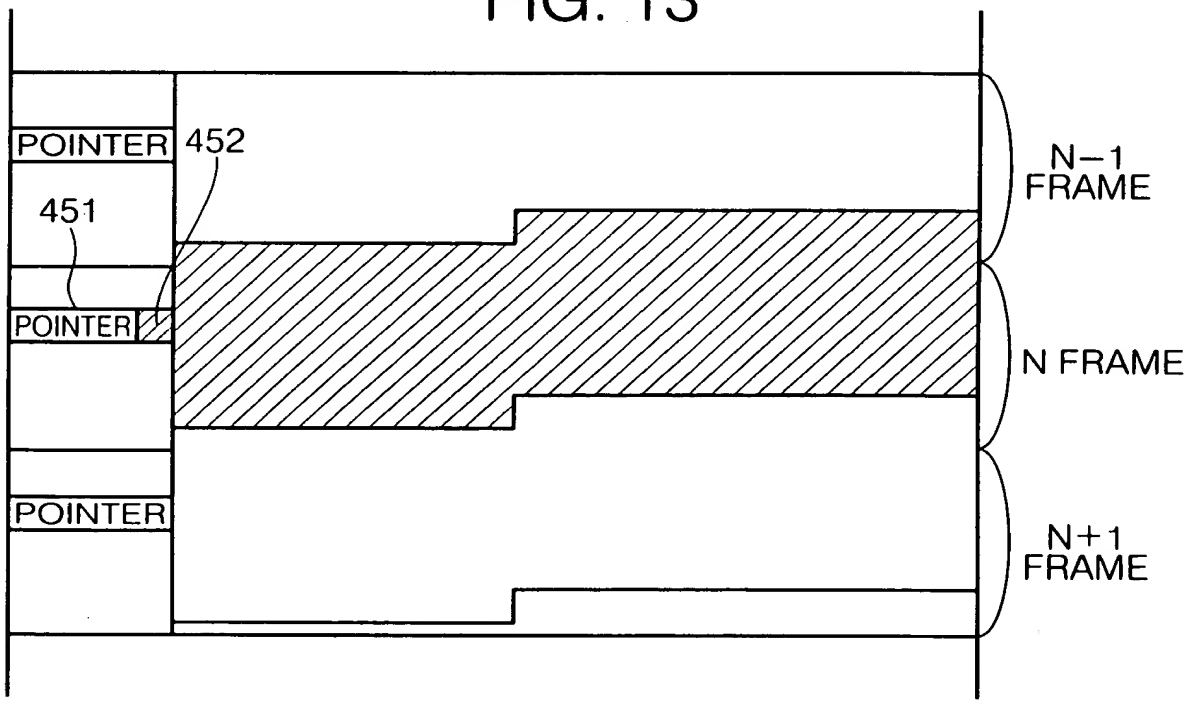
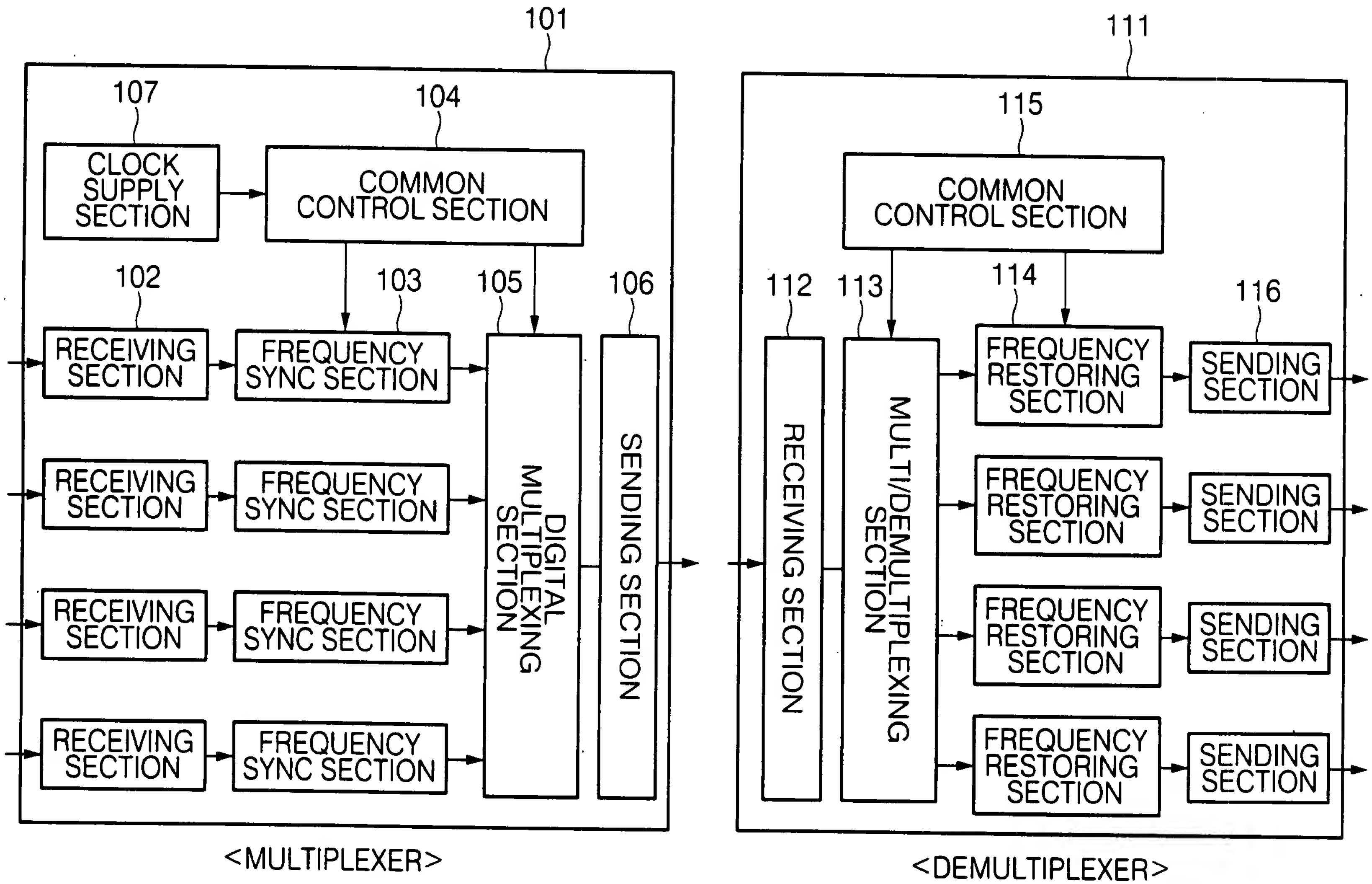

POINTER
452
451
POINTER
POINTER
N−1
FRAME
N FRAME
N+1
FRAME

FIG. 14



101
107
CLOCK SUPPLY SECTION
104
COMMON CONTROL SECTION
102
103
105
106
RECEIVING SECTION
FREQUENCY SYNC SECTION
RECEIVING SECTION
FREQUENCY SYNC SECTION
RECEIVING SECTION
FREQUENCY SYNC SECTION
RECEIVING SECTION
FREQUENCY SYNC SECTION
DIGITAL MULTIPLEXING SECTION
SENDING SECTION
<MULTIPLEXER>
111
115
COMMON CONTROL SECTION
112
113
114
116
RECEIVING SECTION
MULTI/DEMULTIPLEXING SECTION
FREQUENCY RESTORING SECTION
SENDING SECTION
FREQUENCY RESTORING SECTION
SENDING SECTION
FREQUENCY RESTORING SECTION
SENDING SECTION
FREQUENCY RESTORING SECTION
SENDING SECTION
<DEMULTIPLEXER>

FIG. 15

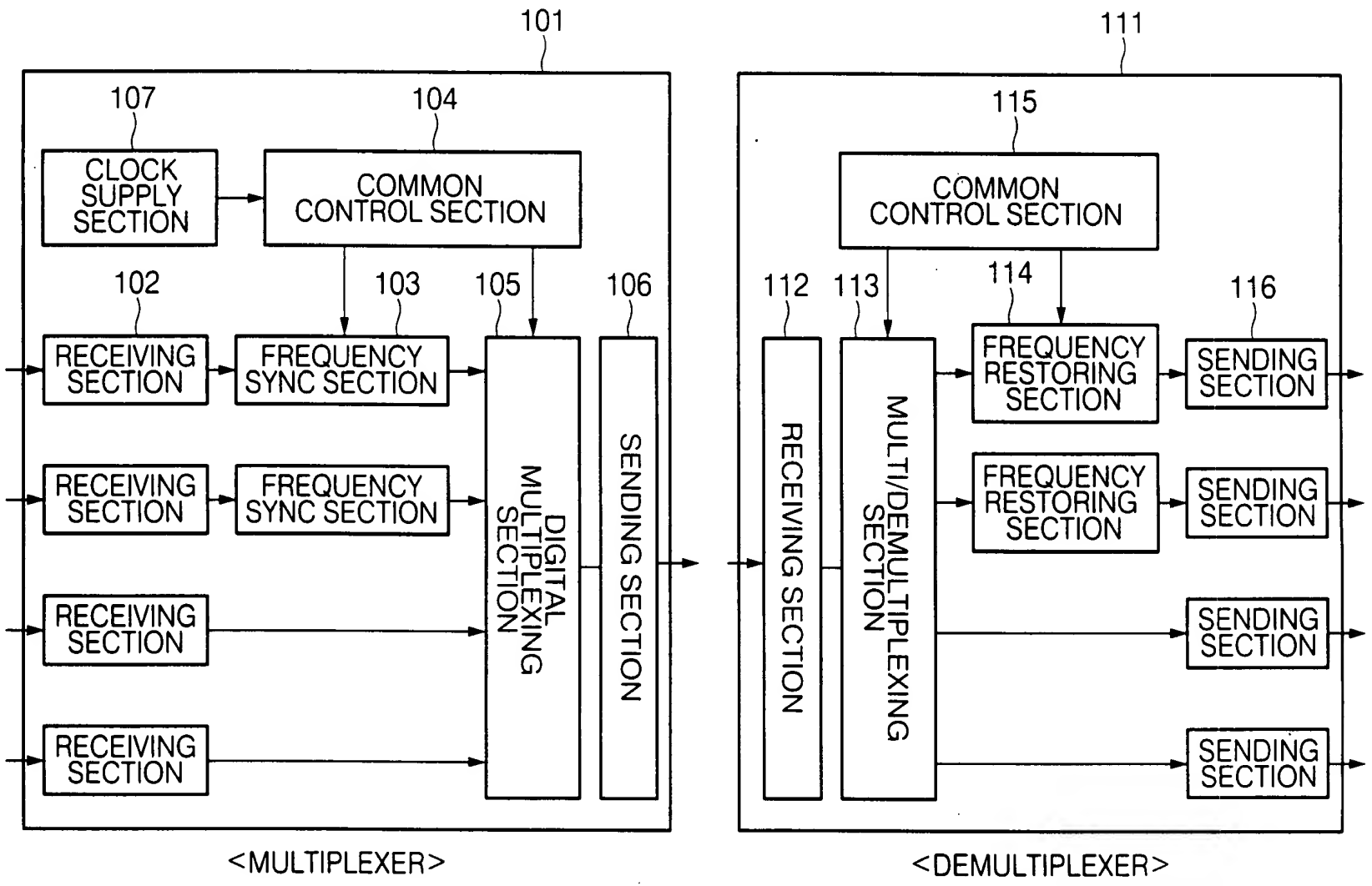

101
107
104
CLOCK SUPPLY SECTION
COMMON CONTROL SECTION
102
103
105
106
RECEIVING SECTION
FREQUENCY SYNC SECTION
RECEIVING SECTION
FREQUENCY SYNC SECTION
RECEIVING SECTION
RECEIVING SECTION
DIGITAL MULTIPLEXING SECTION
SENDING SECTION
<MULTIPLEXER>
111
115
COMMON CONTROL SECTION
112
113
114
116
RECEIVING SECTION
MULTI/DEMULTIPLEXING SECTION
FREQUENCY RESTORING SECTION
FREQUENCY RESTORING SECTION
SENDING SECTION
SENDING SECTION
SENDING SECTION
SENDING SECTION
<DEMULTIPLEXER>

FIG. 16

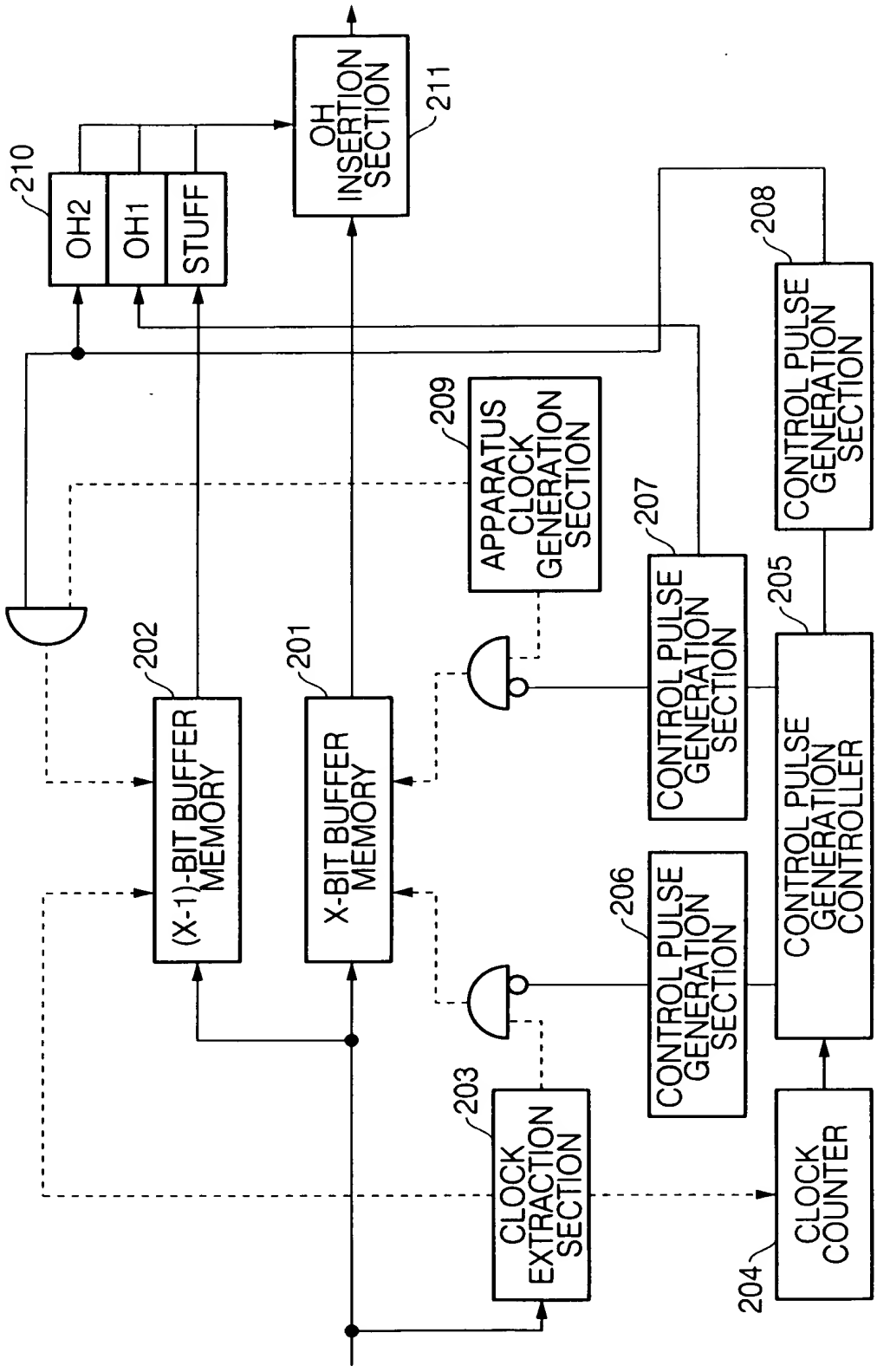

OH2
OH1
STUFF
210
OH INSERTION SECTION
211
APPARATUS CLOCK GENERATION SECTION
209
CONTROL PULSE GENERATION SECTION
208
(X-1)-BIT BUFFER MEMORY
202
X-BIT BUFFER MEMORY
201
CONTROL PULSE GENERATION SECTION
207
CONTROL PULSE GENERATION CONTROLLER
205
CONTROL PULSE GENERATION SECTION
206
CLOCK EXTRACTION SECTION
203
CLOCK COUNTER
204

FIG. 17

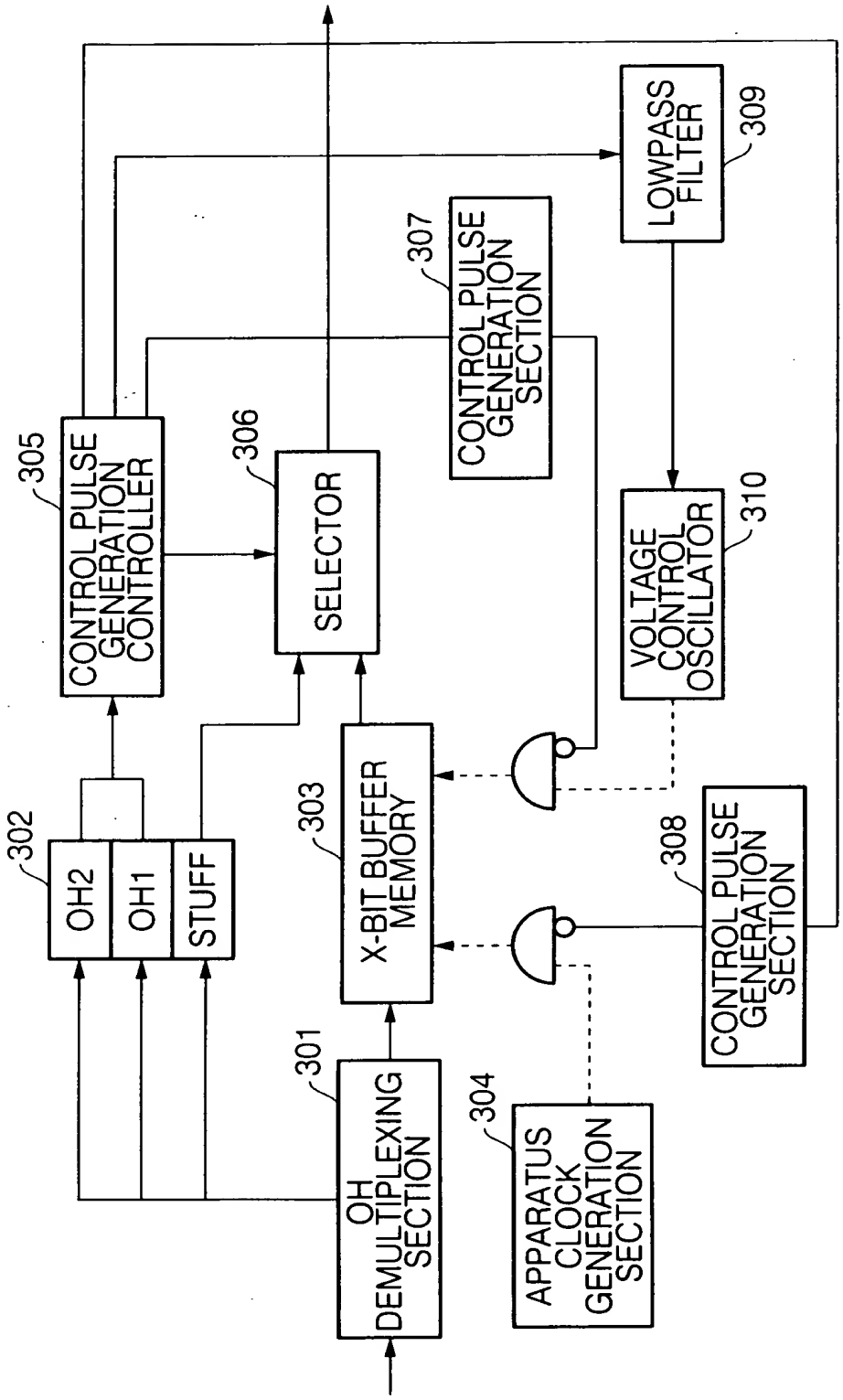

OH DEMULTIPLEXING SECTION
301
OH2
OH1
STUFF
302
X-BIT BUFFER MEMORY
303
APPARATUS CLOCK GENERATION SECTION
304
CONTROL PULSE GENERATION CONTROLLER
305
SELECTOR
306
CONTROL PULSE GENERATION SECTION
307
CONTROL PULSE GENERATION SECTION
308
LOWPASS FILTER
309
VOLTAGE CONTROL OSCILLATOR
310

FIG. 18

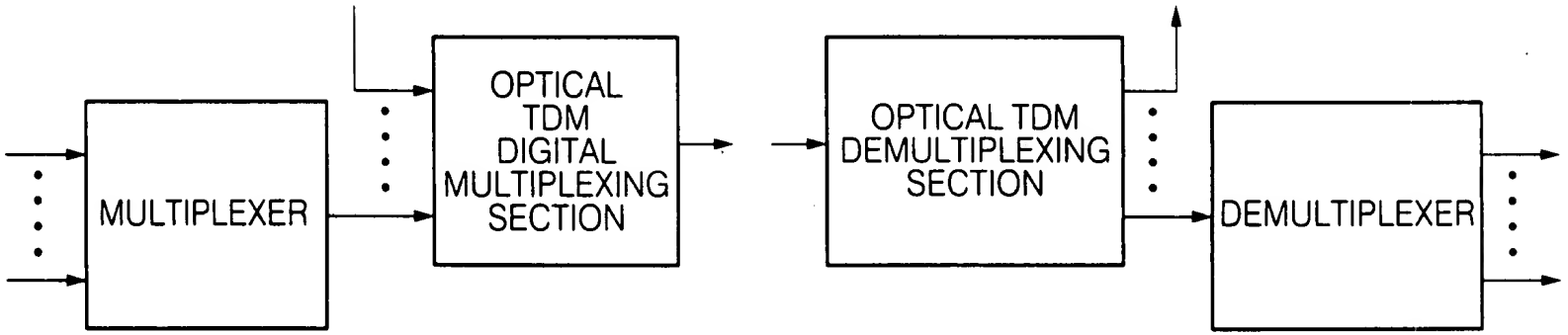
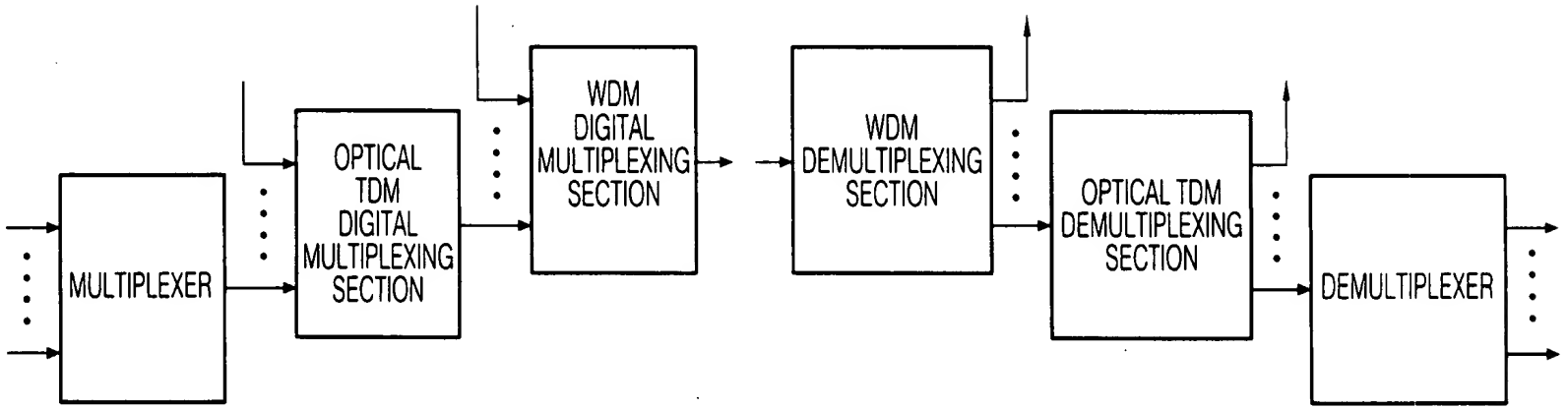

MULTIPLEXER
OPTICAL TDM DIGITAL MULTIPLEXING SECTION
OPTICAL TDM DEMULTIPLEXING SECTION
DEMULTIPLEXER

FIG. 19


MULTIPLEXER
OPTICAL TDM DIGITAL MULTIPLEXING SECTION
WDM DIGITAL MULTIPLEXING SECTION
WDM DEMULTIPLEXING SECTION
OPTICAL TDM DEMULTIPLEXING SECTION
DEMULTIPLEXER